**Low Sampling**

S: In semiconductor development, there is usually a trade off between yield and device performance. Taller gate height = less leakage = better performance but closer to metal contact = less yield. As part of my job I have to weigh whether the yield implications is worth the performance improvement.

T: There was one change that was supposed to drive our device performance up significantly. We ran a small sample with this change and it showed 5% yield degrade in SRAM which was very significant. Team convinced this change was too detrimental to yield and therefore the change should not be considered. I wasn’t convinced because the sample size was so small so I made it my task to convince my coworkers to give me more time to work with the data.

A: I argued that since this change wasn’t currently in production, we can spend more time looking at it more deeply. If I was wrong, then we won’t lose much and the process change just won’t go through. However, if I was right and we don’t proceed with the change, we can be missing out on significant performance improvements. I did a deep dive into the wafers and my hunch was that with a small sample size, it is very possible that there can be some sort of selection bias going on. I ran the impacted wafers through an algorithm I wrote and found that all of these wafers went through a specific tool on a specific process step. On closer look, all wafers that went through this tool had lower yield. I communicated my results and asked for another split lot but this time avoiding that tool.

R: The results showed no statistically significant difference in yield and not only did I get a beneficial change passed, I also found a tool that was impacting yield and needed maintenance.

**Berkeley and Work**

S: About a year after I started working at IBM, I noticed that data science and machine learning is very applicable at my work but also completely underutilized. Because of this, I decided to expand my knowledge and with my boss’s blessing IBM, paid for my degree at UC Berkeley.

T: However, more than once, I’ve had multiple final projects coincide with a busy work week which left me feeling overwhelmed by all I had to do.

A: My approach to this amount of stress was to focus on what I can control, break the problem down into smaller achievements, a lot of time management, and good communication with my teammates and manager as well as prioritizing my tasks.

R: Although it was a very difficult journey, I was able to graduate from UC Berkely with a 4.0 GPA while actually overperforming at my work because I was able to utilize all the new skills I’ve learned.

**Patent Application**

S: A few of my coworkers and I came up with a good idea for a patent, so we would meet a few times a week to write it out.

T: Because everyone had a busy schedule most of my coworkers were either hesitant to take on the tedious task of writing out the patent or were not knowledgeable enough about the process flow.

A: I took it upon myself to write out the patent as well as create all the images illustrating the process flow to create our invention.

R: The patent team at IBM were very excited about our patent and we got it published as top priority. Also because I put in so much work, my coworkers unanimously agreed to have my name first as the publishing author of the patent.

**Transformation Policy**

S: Our team had a big push towards analysis with python and dashboard building called the transformation era. During this time management made a big push for all engineers to learn python and create dashboards to automate their work.

T: I personally disagreed with this policy because I felt it was unfair to a lot of engineers who have their own ways of doing their work and either are not able to or don’t want to learn a skill like python and dashboard creation.

A: However, once the policy has been set, I did my best to help my coworkers. As someone who coded regularly in python, I held education sessions to help people get set up and I went over all the basics of dashboard creation. I also opened my doors as the expert of the team for whoever needs my help.

R: In the end, our engineers gained a valuable new skill and some of them actually became very good at creating dashboards which generated a lot of value for themselves and IBM.

**Presenting Fin Res Metric to VP**

S: Shortly after I started my degree at Berkeley, I created my first machine learning model to classify a certain defect.

T: It was the first time anyone has done this and my manager was so impressed he tasked me to present my model to the VP of the Systems team at IBM.

A: With a lot of guidance and preparation, I did my presentation for my manager, his manager, his manager’s manager, and every gave me a lot of useful input that I took into consideration for my final presentation. I ended up making my presentation result driven, clearly stating what the problem was, what I did and why it was novel and the value it brought to the company. I also had to be careful because the project was very technical and I had to communicate it in a way that was simple enough to understand for a broader audience.

R: After my presentation, the VP of the Systems group was so impressed, there was a big push to utilize machine learning in the hardware development team and it kickstarted the “transformation” project.

**Step up, split second decision**

S: I used to run a department meeting for my second line manager. This meeting was for senior engineers and various other managers and the idea was for me to essentially host the meeting and take notes so that I can get exposed to a lot of higher level decision making conversations that I wouldn’t be exposed to otherwise.

T: One day my second line manager was running late and after 5 minutes of waiting for her to show up, I had to make the decision to start and run the meeting myself. I was nervous but I’ve hosted enough of these meetings already to know the usual topics so I took charge of the meeting until my second line manager arrived.

R: After the meeting she told me she really appreciated me taking the lead for the meeting and she was impressed by me stepping up.

**Greg Conflict**

S: I was tasked by management to build a dashboard to handle all the reliability data. The goal was to automate most of the data analysis work as well as offering a portal for management to get a break down of the general reliability health.

T: I could sense that the coworker who was in charge of looking at reliability data was upset about this because he may have felt like his responsibilities are being taken away and I’m stepping on his toes.

A: I wanted to make sure that he felt involved in this project and it was as much his project as it was mine. I held many meetings with him to consistently get his input and during the progress report meetings with management I would go out of my way to give him credit so that he feels appreciated and has pride in how the project turns out.

R: In the end, there was no conflict between me and my coworker and he was very pleased with the results of the dashboard because it made his life much easier. He also wanted to learn how to build a dashboard of his own.

**Fin Res**

S: There was a systematic defect that was consistently reducing our SRAM yield by 5 to 10%. We know exactly what the fail looks like on our SRAM monitoring metrics but we can’t find the root cause.

T: I have just started at UC Berkeley and decided to apply what I’ve learned to solve the problem.

A: I built a classification model with our SRAM parametric data which was able to accurately identify these defects on all our historical and new wafers (I even accounted for false positives and false negatives while tuning my model to get the best possible results). With this new data, I was able to run mass correlations against lots of other parameters and explore different ways to look at the data. By doing this, I was able to find a slot order dependence on a specific RIE process step and that the vast majority of bad wafers went through a certain tool in that process step.

R: As a result, we were able to decommission that tool, and implement a FOUP purge before that step and the defect went away.

**Ghost Fin**

S: There was a systematic defect that was consistently taking out 4 edge chips on our Logic macro which translated to higher yield loss in the product chips.

T: I was in charge of SRAM and Logic health so it was my responsibility to diagnose this issue.

A: I did a deep dive on the problem and noticed it only affected a certain type of latch. I consulted the expert on the Logic layout and we found that these defects only occurred when we have a 2 Fins with a 4Fin RX below it. We found out that those 4fin RX will shift up or down, depending on top or bottom edge, causing an incomplete etch of the gate, leading to a short. I built a metric to not only classify these defects, but also assign a metric to how bad they were. It was a very difficult issue to fix so we needed a way to track and measure our improvement.

R: After many proposed fixes to the problem, we eventually irradicated the issue.

**Shift Detection**

S: There was an issue on the product chip that we found that could’ve been flagged by a device parameter earlier in the line. One of our senior engineers brought up the question – “why didn’t we notice it sooner?” the answer was that no one was monitoring this parameter because it was so obscure and we had thousands of parameters.

T: I took it upon myself to build a shift detection monitor that would be able to look through all our parameters and notify us if there were any permanent shifts.

A: I did a lot of research and testing and landed on the PELT algorithm for detecting shifts.

R: Not a lot of buy in because I had to do a lot of manual work. Look at the shifted parameters, put together a report and send it to the experts to look at took too much time. I realized my error of not doing a design thinking session to plan out how my potential customers would use this tool. To make up for the error, I did a design thinking session and revamped the workflow of my tool so that it would filter out the most significant shifts, put it on a dashboard with well labeled graphs as well and email notifications to the corresponding experts.

**Clustering Project**

S: During my down time I came up with a cool idea to do wafer clustering based on chip x/y data. I was inspired by a paper written in ieee utilizing this method called Simultaneously Orthogonal Matching Pursuit specifically with wafer regionality data for clustering and I wanted to attempt to build it.

T: During times when I wasn’t busy with other work, I organized a design thinking session for my team to see what potential customers would want to see out of this project. Then I started coding. The paper was a lot harder to understand in terms of the math that was done, so I went above and beyond by finding the author of the paper on linkedin and setting up a few phone calls so he can teach me about the algorithm.

A: I managed to successfully build the clustering algorithm and it worked very well for simple obvious cluster groups. However, if you added complexity to the problem, the clustering algorithm’s performance would deteriorate.

R: I was disappointed by the end capabilities of the tool, but I was proud that I went above and beyond to contact the author of the paper and spent a lot of my free time passionately pursuing a project for work. I also ended up building something no one else on my team managed to build and I learned a lot.

**Vmin Yield Loss**

S: There was a process change that made our pfet devices slightly hotter. One impact of this change that we didn’t expect was a significant Logic Vmin yield degrade. We had run experiments before and this never showed up.

T: I was charged with the difficult task of figuring out why this is the case and if we need to roll back the process change. This was a business critical decision and an urgent one because the yield degrade may significantly impact our cost.

A: I did a lot of analysis and found that the yield loss mainly came from the hottest regions of the wafer and there is a strong correlation between the yield degrade and the idd standby current. This all pointed towards rolling back the change. However, the correlation just didn’t make sense to me so I kept looking and found that the yield loss were coming from blocks 1,2,3, 26,27,28 which were on the ends of our logic macro. These were not the same types of latches so it made no sense that they were failing together. There must be a pattern there. I spend a lot of time looking closely at our logic blueprints and came up with a theory that we had voltage pads extending the logic macro. However, we these voltage boosting pads did note extend to the far ends of the macro and maybe we are being hit by some kind of voltage droop at the ends of the logic macro at our Vmin corner. I knew that this would be a test macro specific problem and would not show up at our later metal layers. To confirm this, I asked an engineer to retest some bad wafers at a later metal layer and noticed that the problem disappeared.

R: This confirms that the issue will not impact our product yield down the line and we do not need to roll back any process changes.

**Chidu**

S: There is one higher up who is not my direct manager but he was a tech leader in semiconductor physics but has very little knowledge in machine learning and building tools with the data. He would have a lot of big project ideas that were not carefully thought out that he would come to me for. I found this a little annoying.

T: However, I realized that it’s because this guy has a lot of project ideas that puts him in this senior position to begin with and the fact that he keeps coming to me means he has evaluation of my capabilities.

A: From him, I learned to be patient and communicate when I think an idea is too vague or unfeasible. However, I also took time to sit down with him and plan out certain ideas in more detail.

R: It was thanks to him that I ended up building multiple classification models for different defects as well as a product yield predictor and pareto ranking tool on one of my dashboards.